

What is claimed is:

- 1 1. An apparatus comprising:
2 an input circuit coupled to a first bus to transfer a delayed
3 transaction (DT) data having a transaction identifier to one of N buffers,
4 the input circuit being dynamically configured according to a bus
5 frequency, N being a positive integer, the one of the N buffers being
6 associated with the transaction identifier; and
7 an output circuit coupled to the buffers to transfer the DT data from
8 the one of the N buffers to a second bus operating at the bus frequency, the
9 output circuit being dynamically configured according to the bus
10 frequency.
- 1 2. The apparatus of claim 1 wherein the input circuit comprises:
2 a 1-to-N de-multiplexing circuit to transfer the DT data from the
3 first bus to the one of the N buffers based on the transaction identifier.
- 1 3. The apparatus of claim 2 wherein the output circuit comprises:
2 a N-to-1 multiplexing circuit to transfer the DT data from the one
3 of the N buffers to the second bus based on the transaction identifier.
- 1 4. The apparatus of claim 3 wherein the 1-to-N de-multiplexing
2 circuit comprises:
3 a 1-to-P de-multiplexer to transfer the DT data to one of P signal
4 paths, P being a positive integers; and

5 P 1-to-Q de-multiplexers coupled to the P signal paths, Q being
6 equal to N/P, each of the 1-to-Q de-multiplexers being coupled to Q of the
7 N buffers to transfer the DT data to one of the Q buffers based on the
8 transaction identifier.

1 5. The apparatus of claim 4 wherein each of the P 1-to-Q de-
2 multiplexers transfers the DT data to the one of the Q buffers alternately.

1 6. The apparatus of claim 3 wherein the N-to-1 multiplexing circuit
2 comprises:

3 P Q-to-1 multiplexers coupled to Q of the N buffers to transfer the
4 DT data from one of the Q buffers to P signal paths based on the
5 transaction identifier; and

6 a P-to-1 multiplexer coupled to the P Q-to-1 multiplexers via the P
7 signal paths to transfer the DT data to the second bus.

1 7. The apparatus of claim 6 wherein each of the P Q-to-1 multiplexers
2 transfers the DT data to the one of the Q buffers alternately.

1 8. The apparatus of claim 1 wherein the first bus is a primary bus
2 coupled to a memory.

1 9. The apparatus of claim 1 wherein the second bus is one of a
2 Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

1 10. The apparatus of claim 9 wherein the delayed transaction data
2 corresponds to a split transaction data when the second bus is the PCI-X bus.

1 11. A method comprising:
2 transferring a delayed transaction (DT) data having a transaction
3 identifier to one of N buffers using an input circuit coupled to a first bus,
4 the input circuit being dynamically configured according to a bus
5 frequency, N being a positive integer, the one of the N buffers being
6 associated with the transaction identifier; and
7 transferring the DT data from the one of the N buffers to a second
8 bus operating at the bus frequency using an output circuit, the output
9 circuit being dynamically configured according to the bus frequency.

1 12. The method of claim 11 wherein transferring the DT data to the
2 one of N buffers comprises:
3 transferring the DT data from the first bus to the one of the N
4 buffers based on the transaction identifier using a 1-to-N de-multiplexing
5 circuit.

1 13. The method of claim 12 wherein transferring the DT data from the
2 one of the N buffers comprises:
3 transferring the DT data from the one of the N buffers to the
4 second bus based on the transaction identifier using a N-to-1 multiplexing
5 circuit.

1 14. The method of claim 13 wherein transferring the DT data using the
2 1-to-N de-multiplexing circuit comprises:
3 transferring the DT data to one of P signal paths using a 1-to-P de-
4 multiplexer, P being a positive integers; and

5 transferring the DT data to one of Q of the N buffers based on the
6 transaction identifier using P 1-to-Q de-multiplexers coupled to the P
7 signal paths, Q being equal to N/P, each of the 1-to-Q de-multiplexers
8 being coupled to the Q buffers.

1 15. The method of claim 14 wherein transferring the DT data to one of
2 the Q buffers comprises transferring the DT data to the one of the Q buffers
3 alternately using each of the P 1-to-Q de-multiplexers.

1 16. The method of claim 13 wherein transferring the DT data from the
2 one of the N buffers using the N-to-1 multiplexing circuit comprises:

3 transferring the DT data from one of the Q buffers to P signal paths
4 based on the transaction identifier using P Q-to-1 multiplexers coupled to
5 Q of the N buffers; and

6 transferring the DT data to the second bus using a P-to-1
7 multiplexer coupled to the P Q-to-1 multiplexers via the P signal paths.

1 17. The method of claim 16 wherein transferring the DT data to the
2 second bus using a P-to-1 multiplexer comprises transferring the DT data to the
3 one of the Q buffers alternately using each of the P Q-to-1 multiplexers.

1 18. The method of claim 11 wherein the first bus is a primary bus
2 coupled to a memory.

1 19. The method of claim 11 wherein the second bus is one of a
2 Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

1 20. The method of claim 19 wherein the delayed transaction data
2 corresponds to a split transaction data when the second bus is the PCI-X bus.

1 21. A system comprising:
2 a processor having a host bus;
3 a memory having a first bus;
4 a chipset coupled to the processor via the host bus and the memory
5 via the first bus to control accesses to the memory from a device via a
6 second bus operating at a bus frequency, the chipset having a buffer
7 circuit, the buffer circuit comprising:
8 an input circuit coupled the a first bus to transfer a delayed
9 transaction (DT) data having a transaction identifier to one of N buffers,
10 the input circuit being dynamically configured according to the bus
11 frequency, N being a positive integer, the one of the N buffers being
12 associated with the transaction identifier, and
13 an output circuit coupled to the buffers to transfer the DT data from
14 the one of the N buffers to the second bus, the output circuit being
15 dynamically configured according to the bus frequency.

1 22. The system of claim 21 wherein the input circuit comprises:
2 a 1-to-N de-multiplexing circuit to transfer the DT data from the
3 first bus to the one of the N buffers based on the transaction identifier.

1 23. The system of claim 22 wherein the output circuit comprises:
2 a N-to-1 multiplexing circuit to transfer the DT data from the one
3 of the N buffers to the second bus based on the transaction identifier.

1 24. The system of claim 23 wherein the 1-to-N de-multiplexing circuit
2 comprises:

3 a 1-to-P de-multiplexer to transfer the DT data to one of P signal
4 paths, P being a positive integers; and

5 P 1-to-Q de-multiplexers coupled to the P signal paths, Q being
6 equal to N/P, each of the 1-to-Q de-multiplexers being coupled to Q of the
7 N buffers to transfer the DT data to one of the Q buffers based on the
8 transaction identifier.

1 25. The system of claim 24 wherein each of the P 1-to-Q de-
2 multiplexers transfers the DT data to the one of the Q buffers alternately.

1 26. The system of claim 23 wherein the N-to-1 multiplexing circuit
2 comprises:

3 P Q-to-1 multiplexers coupled to Q of the N buffers to transfer the
4 DT data from one of the Q buffers to P signal paths based on the
5 transaction identifier; and

6 a P-to-1 multiplexer coupled to the P Q-to-1 multiplexers via the P
7 signal paths to transfer the DT data to the second bus.

1 27. The system of claim 26 wherein each of the P Q-to-1 multiplexers
2 transfers the DT data to the one of the Q buffers alternately.

1 28. The system of claim 21 wherein the second bus is one of a
2 Peripheral Component Interconnect (PCI) bus and a PCI-X bus.

- 1 29. The system of claim 28 wherein the delayed transaction data
2 corresponds to a split transaction data when the second bus is the PCI-X bus.